

direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes; and

*Concluded  
B1*  
a peripheral circuit section for selectively writing information into or reading information from the memory cell,

wherein the memory cell array and the peripheral circuit section are disposed in different layers,

wherein the peripheral circuit section is formed in a region outside the memory cell array, and

wherein the ferroelectric layer is disposed linearly along the first signal electrodes or the second signal electrodes.

#### REMARKS

Claims 1-49 are pending. Claims 24-49 have been previously withdrawn from consideration.

Applicants gratefully acknowledge that the Office Action indicates that claims 4-8, 10, 11, 13-18, 20 and 23 would be allowable if rewritten in independent form.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Reconsideration based on the following remarks is respectfully requested.

I. The Specification Satisfies All Formal Requirements

The Office Action objects to the Title based on informalities. The Title is amended to obviate this objection. Withdrawal of the objection to the Title is respectfully requested.

II. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1-3, 9, 19, 21 and 22 under 35 U.S.C. §102(b) over Nagasaki et al. (U.S. Patent No. 5,060,191); and claim 12 under 35 U.S.C. §103(a) over